AF
2800

#17
Amdt
D
(WE)
9-3-02

AMENDMENT AFTER FINAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

HIKITA et al.

Art Unit: 2827

Application No.: 09/496,183

Examiner: CRUZ, L.

Filed: February 2, 2000

Attorney Dkt. No.: 103213-09038

For: SEMICONDUCTOR DEVICE AND SEMICONDUCTOR CHIP FOR USE THEREIN

AMENDMENT AFTER FINAL UNDER 37 CFR § 1.116

Commissioner for Patents
Washington, D.C. 20231
BOX: AF

August 21, 2002

Sir:

In response to the outstanding Office Action dated May 21, 2002, please amend the application as follows:

IN THE CLAIMS:

Please cancel claims 8-9 without prejudice or disclaimer.

Please amend claims 1, 3 and 10 as follows:

1. (Thrice Amended) A semiconductor device comprising a first semiconductor chip and a second semiconductor chip superposed on and bonded to a surface of the first semiconductor chip,

wherein, in a chip bonding region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, chip

connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips,

wherein, on the second semiconductor chip, chip connection portions are arranged so as to fit the chip connection portions arranged on the first semiconductor chip at least for one of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along a first side of said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along said first side of said at least one pair of opposite sides to the chip connection portions arranged along a second side of said at least one pair of opposite sides, and at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

3. (Thrice Amended) A semiconductor chip having, on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips,

wherein, in the chip bonding region, chip connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along a first side of said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along said first side of said at least one pair of opposite sides to the chip connection portions arranged along a second side of said at least one pair of opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

10. (Thrice Amended) A semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips,

wherein, in the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are arranged along an edge of the chip connection region, and

wherein the chip connection portions are arranged along at least one pair of opposite sides of the chip connection region, a distance between the chip connection portions arranged along a first side of said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along said first side of said at least one pair of opposite sides to the chip connection portions arranged along a second side of said at least one pair of opposite sides, and at least part of the chip

connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

REMARKS

The Office Action dated May 21, 2002 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 8-9 have been cancelled without prejudice or disclaimer. Claims 1, 3 and 10 have been amended. No new matter has been added. The amendments are cosmetic in nature only and do not narrow the scope of any elements of any claims, and no new issues are raised which require further search or consideration. Accordingly, Claims 1-5 and 10-11 are pending in this application and are submitted for consideration. Entry of this Amendment is earnestly requested.

Claims 1-5 and 10-12 were rejected under 35 U.S.C. § 112, second paragraph as indefinite. In particular, the phrase "the other" was found to lack antecedent basis. Independent claims 1, 3 and 10 are amended herein to clarify the patented configuration. In particular, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region. A distance between the chip connection portions arranged along a first side of said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along said first side of said at least one pair of opposite sides to the chip connection portions arranged along a second side of said at least one pair of opposite sides, and at least part of the chip connection portions arranged on the

first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications. Therefore, Applicants submit that claims 1-5 and 10-12 comply with the requirements of 35 U.S.C. § 112., and request that the rejection be withdrawn.

Claims 1-5 and 10-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wenzel et al. (U.S. Patent No. 6,150,724, hereinafter "Wenzel"). Claim 12 was cancelled in the response dated March 12, 2002. As for claims 1-5, 10 and 11, Applicants respectfully traverse the rejection and submit that each of these claims, as submitted herein, recites subject matter that is not disclosed by Wenzel.

Claim 1, upon which claim 2 is dependent, recites a semiconductor device comprising a first semiconductor chip and a second semiconductor chip superposed on and bonded to a surface of the first semiconductor chip. In a region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, the chip connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips. In addition, on the second semiconductor chip, the chip connection portions are arranged so as to fit the chip connection portions arranged on the first semiconductor chip at least for one of the plurality of predetermined types of semiconductor chips. Furthermore, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region. A distance between the chip connection portions arranged along a first side of the opposite sides of at least one pair of opposite sides, is shorter than a distance from the chip connection portions arranged along the first side of the opposite sides of the pair to the chip connection portions

arranged along as second side of the opposite sides of the pair. Also, at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Claim 3, upon which claims 4-5 are dependent, recites a semiconductor chip having, on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips. In the chip bonding region, the chip connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips. Furthermore, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region. A distance between the chip connection portions arranged along a first side of the opposite sides of at least one pair of opposite sides, is shorter than a distance from the chip connection portions arranged along the first side of the opposite sides of the pair to the chip connection portions arranged along as second side of the opposite sides of the pair. Also, at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Claim 10, upon which claims 11-12 are dependent, recites a semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips. In the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are

arranged along an edge of the chip connection region. Furthermore, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region. A distance between the chip connection portions arranged along a first side of the opposite sides of at least one pair of opposite sides, is shorter than a distance from the chip connection portions arranged along the first side of the opposite sides of the pair to the chip connection portions arranged along as second side of the opposite sides of the pair. Also, at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Accordingly, the present invention provides a semiconductor device having a chip-on-chip structure that allows easy production of various types of semiconductor devices as a whole, and further provides a semiconductor chip for use in a semiconductor device. As such, the claimed invention provides an efficient and cost effective method and device for upgrading an existing system, such as increasing the capacity of a memory, increasing the number of conversion bits of A/D conversion device, or increasing the number of processing bits of a CPU.

Wenzel discloses a bump-bonded multi-IC flip-chip semiconductor device 100. The device 100, as illustrated in Figure 5 of Wenzel, has a mother integrated circuit or chip 102 and a daughter integrated circuit or chip 104. The active surface of the mother chip 102, which contains active circuitry, faces the active surface circuitry of the daughter integrated circuit 104. In other words, the active surface of both ICs 102 and 104 are facing one another. The conductive bumps 108 are used to interconnect active

circuitry and interconnect structures located on the mother integrated circuit 102 with active circuitry or conductive structures located on the daughter integrated circuit 104. The interconnected structure of the chips 102 and 104 is coupled to a ceramic, organic, or other package 106 through conductive connection bumps 110. Central bumps 108 are used to connect two or more integrated circuits to each other while peripheral bumps 110 are used to connect the mother chip 102 to the semiconductor package 106 to enable electrical connection of the ICs 102 and 104 to an external environment. Fig. 6 of Wenzel is the only place where an arrangement of chip connection portions is shown from a top view, and clearly, the claimed configuration of chip connection portions, defined by independent claims 1, 3 and 10, is not shown or suggested. In particular, the chip connection portions are equally spaced on the first semiconductor chip within the bonding area.

Applicants submit that Wenzel fails to disclose or suggest chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, wherein a distance between the chip connection portions arranged along a first side of a pair of opposite sides is shorter than a distance from the chip connection portions arranged along the side of the pair of opposite sides to the chip connection portions arranged along a second side of the pair of opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications, as defined by each of the independent claims.

As discussed above, Wenzel merely discloses a bump-bonded multi-chip flip-chip device 100 formed by manufacturing a mother chip 102 having a first set 207 of bumps 212 and a second set 209 of bump contact with conductive bumps 108 used to interconnect activity circuitry and interconnect structures located on the mother integrated circuit 102 with active circuitry or conductive structures located on the daughter integrated circuit 104. Wenzel also fails to disclose at least part of the chip connection portions arranged on the first semiconductor chip are common to a plurality of predetermined types of semiconductor chip. It is respectfully submitted that by using these common chip connection portions, it is possible to achieve connection with a plurality of types of semiconductor chip. Thus, Applicants respectfully submit that Wenzel fails to disclose and suggest each and every element recited in independent claims 1, 3 and 10 of the present application. Accordingly, Applicants request that the rejection be withdrawn and that claims 1, 3 and 10 be allowed.

As for dependent claims 2, 4-5 and 11, Applicants submit that each of these claims recites subject matter which is neither disclosed nor suggested by Wenzel. In particular, each of claims 2, 4-5 and 11 depends from claims 1, 3 and 10, respectively. Thus, Applicants submit that Wenzel fails to teach each and every element of claims 2, 4-5 and 11. Applicants request that the rejection be withdrawn and that claims 2, 4-5 and 11 be allowed.

In view of the above, Applicants respectfully submit that claims 1-5 and 10-11, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully

request that claims 1-5 and 10-11 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicants' undersigned Attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

Brian A. Tollefson
Attorney for the Applicants
Registration No. 46,338

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

BAT:ccd